APPLICATION FOR UNITED STATES PATENT

by

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for

INSULATOR STRUCTURE AND METHOD FOR PRODUCING INSULATOR STRUCTURES IN A SEMICONDUCTOR SUBSTRATE

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INSULATOR STRUCTURE AND METHOD FOR PRODUCING INSULATOR STRUCTURES IN A SEMICONDUCTOR SUBSTRATE

BACKGROUND

FIELD

[0001] The invention relates to methods for producing insulator structures in a semiconductor substrate, in which insulator trenches are introduced into the semiconductor substrate from a substrate surface of the semiconductor substrate, and furthermore relates to an insulator structure.

BACKGROUND INFORMATION

[0002] In semiconductor process technology, dimensions of semiconductor devices fabricated on or in a semiconductor substrate (wafer) are continually being reduced in order to increase a yield of semiconductor devices per wafer, and to reduce a response time or a power consumption of the semiconductor devices.

[0003] In the course of processing semiconductor devices in a wafer, a sequence of process steps for shaping insulator structures is effected in a process module. For instance, insulator structures isolate interconnects arranged in an identical metallization plane electrically from one another (intermetal dielectric, IMD) or insulate conductive sections formed below a substrate surface of the semiconductor substrate from one another (shallow trench isolation, STI). In this case, the conductive sections are doped sections of the semiconductor substrate that are formed, for example, as source/drain regions of transistors, or as structures made of conductive material that are introduced into the semiconductor substrate, such as connecting lines and electrodes of capacitor structures made of doped polysilicon.

[0004] A customary insulator material for fabricating the insulator structures is silicon oxide. In this case, the silicon oxide is preferably deposited by means of a deposition process based on a high density plasma (high density plasma, chemical vapor deposition, HDP/CVD). Silicon oxide layers of high conformity are produced by means of the HPD/CVD deposition process. Insulator structures formed from such silicon oxide layers have a high density and a high quality.

[0005] Toward smaller dimensions, insulator structures between interconnects of a metallization plane are increasingly subject to a requirement that a capacitive coupling of adjacent interconnects, which initially rises with a smaller distance, be kept small by the selection of an insulator material having low permittivity (low-k dielectric). U.S. Patent No. 6,375,744 (Murugesh et al.), for instance, discloses methods that reduce the permittivity of the deposited insulator material by the addition of fluorine-containing additives (fluorine-based additives) during the deposition process and the partial incorporation thereof into the insulator material. In this case, it is assumed that additions of electronegative fluorine, for instance, reduce the polarizability of an Si-O-F structure produced in this way and an Si-O-F structure therefore has a lower permittivity or dielectric constant than a silicon oxide without additions. For silicon oxide layers to which fluorine is added, the terms fluorinated silicate glass, FSG) and fluorine-doped silicon oxide film are customary in this context, while in order to distinguish conceptually from this, the term undoped silicon oxide is used if the silicon oxide emerges from chemical precursor compounds (precursors) without halogen components.

[0006] Insulator structures embodied in the semiconductor substrate generally emerge from a process of filling insulator trenches introduced into the semiconductor substrate from a substrate surface. Since structures of active areas formed in the semiconductor substrate are often better scaleable with regard to planar dimensionings than with regard to a vertical dimensioning with respect to the substrate surface, there is an increase in the aspect ratio AR between a depth of the insular trenches and an opening width of the insulator trenches at the substrate surface. It is foreseeable that insulator trenches having an aspect ratio AR > 5:1 will be necessary for minimum feature sizes of less than 100 nanometers.

[0007] A defect-free, complete (void-free) filling of the insulator trenches is made more difficult as the aspect ratio increases. With undoped silicon oxide, using conventional HDP/CVD deposition processes, insulator trenches can be filled essentially in a defect-free manner only up to an aspect ratio of AR < 4.

[0008] U.S. Patent No. 6,372,291 (Hua et al.), for instance, discloses that adding fluorine or a fluorine compound during the deposition process positively influences the filling operation and enables a defect-free, directional filling from the trench bottom even of insulator trenches having an aspect ratio AR > 4:1 to AR < 7:1. It is assumed in this case that the fluorine in the form of free radicals forms an etching component, which counteracts a growth of material in the area of the trench openings and thus an accretion of the insulator trenches in the region of the trench openings before a complete filling of a lower trench region (sputtering). Consequently, the insulator trenches are filled directionally from the trench bottom (bottom-up fill).

[0009] If an insulator trench introduced in a semiconductor substrate is filled in the manner described, then an interaction disadvantageously occurs between fluorine that is outgassing or outdiffusing from the doped silicon oxide and the material of the semiconductor substrate, typically monocrystalline silicon. On account of the interaction, a low-quality oxide arises in the insulator structure along an interface with the semiconductor substrate. The low-quality oxide has, in comparison with the insulator material, a lower etching resistance that is altered with respect to customary etching processes.

[0010] Figure 1 diagrammatically illustrates a cross-section of two insulator trenches 21 introduced into a semiconductor substrate 1 on both sides of a web 22 formed by the semiconductor substrate 1. A residual section of a protective layer 11, which is necessary for a previous processing, is arranged on the web 22. The insulator trenches 21 are filled with an insulator filling 3, which is deposited in the course of an HDP/CVD deposition process and extends beyond a substrate surface 11. Facets 30 which are typical of the HDP deposition process form above the webs 22. The material of the insulator filling 3 is fluorine-doped silicon oxide. Fluorine outgasses or outdiffuses from the insulator filling 3. At the interface with the web 22, defect areas 6 form on account of an interaction of the fluorine with the silicon of the semiconductor substrate. The silicon oxide of the insulator filling 3 is of low quality in the defect areas 6.

[0011] Usually, after the filling of the insulator trenches, insulator material deposited above the substrate surface in the course of the HDP/CVD deposition process is planarized, for instance by means of a chemical mechanical polishing method (CMP).

The low-quality oxide in the defect areas is also attacked during subsequent etchings. The insulator structure is consequently caused to recede below the substrate surface in the defect areas.

[0012] After the removal of the insulator material from the sections arranged above the substrate surface, the insulator structure formed in the insulator trench has gaps at the interfaces with the semiconductor substrate. The gaps may be filled with conductive materials in subsequent process steps, for instance during the formation of conductive structures, and consequently be the cause of short circuits.

[0013] A short circuit attributable to a defect area 6 is illustrated diagrammatically in plan view in Figure 2. The defect area 6 extends in an insulator trench 21 along a web 22 made of crystalline silicon. An insulator material filling the insulator trenches 21 is caused to recede as far as a substrate surface. Two gate conductor structures formed in each case from a gate conductor (GC) are arranged on the substrate surface and, by way of example, form mutually insulated word lines for driving transistors 73 formed in active areas 7 (AA). For this purpose, the gate conductor was deposited in areal fashion and patterned by means of an etching step. Sections of the gate conductor bearing on the substrate surface between the gate conductor structures 72 were removed during the etching step. Residual portions of the gate conductor remain in the defect area 6 below the substrate surface and consequently short-circuit the two gate conductor structures 72.

[0014] It is furthermore known that defect areas with low-quality oxide do not arise if fluorine-doped silicon oxide is deposited on a thin silicon nitride layer (nitride liner)

covering the semiconductor substrate. No perceptible interaction of fluorine with the monocrystalline silicon of the semiconductor substrate occurs in this case.

[0015] Figure 3 diagrammatically illustrates a cross section – adapted from a scanning electron microscopy (SEM) recording – through a structure comprising webs 22 and insulator trenches 21 in a semiconductor substrate 1, said structure being covered with a nitride liner 12. The trenches have a depth of 570 nm with a width of about 135 nm. The aspect ratio AR of the insulator trenches 21 is greater than 4:1. No defect areas are discernible. The insulator trenches 21 are filled without any defects.

SUMMARY

[0016] In the processes and structures described above, it is disadvantageous that p-channel transistors that are formed using customary technology in sections of the semiconductor substrate which are covered by a silicon nitride liner applied before the HDP/CVD deposition process have a comparatively high degradation rate in comparison with such p-channel transistors that are not formed on sections of the semiconductor substrate covered with a silicon nitride liner beforehand. As an aspect of the invention, a method is disclosed for producing insulator structures by filling insulator trenches introduced into a semiconductor substrate, in which insulator trenches with a high aspect ratio are filled reliably and completely and a functionality of semiconductor devices that are subsequently formed in the semiconductor substrate remains ensured. Moreover, an insulator structure is disclosed that ensures a functional integrity of the semiconductor devices subsequently formed in the semiconductor substrate, in particular of p-channel transistors.

[0017] Accordingly, a method is disclosed for producing insulator structures in a semiconductor substrate. Insulator trenches are introduced into the semiconductor substrate from a substrate surface of the semiconductor substrate. The insulator trenches are at least partially filled with a main layer made of an additive-doped insulator material in the course of an HDP deposition process based on a high density plasma. A barrier layer, which blocks an interaction of the additive with the semiconductor substrate, is produced before a deposition of the main layer in the course of the HDP deposition process.

[0018] An insulator structure in a semiconductor substrate is also described. The structure includes a main layer, which has been formed from halogen-doped silicon oxide and has emerged from an HDP deposition process. Also featured is a barrier layer, which isolates the main layer from the semiconductor substrate and is formed in direct connection with the main layer by means of an HDP deposition process and blocks an interaction of the halogen with the semiconductor substrate.

[0019] The invention is explained in more detail below with reference to diagrammatic drawings on the basis of preferred exemplary embodiments of the methods according to the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The invention is explained in more detail below with reference to the appended drawings, in which, in detail:

[0021] Figure 1 illustrates a cross section, adapted from an SEM recording and true to scale, through a first insulator structure, processed according to a first known method, in a first process stage.

[0022] Figure 2 is a plan view, also adapted from an SEM recording and true to scale, of the insulator structure processed according to the first known method, in a second process stage.

[0023] Figure 3 illustrates a cross-section, adapted from an SEM recording and true to scale, through an insulator structure processed according to a second known method.

[0024] Figure 4 illustrates a cross-section, adapted from an SEM recording and true to scale, through an insulator structure processed according to a first exemplary embodiment of a method in accordance with the invention.

[0025] Figure 5 illustrates a cross-section, adapted from an SEM recording and true to scale, through an insulator structure processed according to a second exemplary embodiment of the method in accordance with the invention.

[0026] Figure 6 illustrates a cross-section, adapted from an SEM recording and true to scale, through an insulator structure processed according to a third exemplary embodiment of the method in accordance with the invention.

DETAILED DESCRIPTION

[0027] The following reference numerals are used consistently throughout the specification:

1	Semiconductor substrate
10	Substrate surface
11	Protective layer
12	Nitride liner
21	Insulator trench
22	Web
3	Insulator filling
30	Facet
31	Additional layer

32	Barrier layer
33	Main layer
34	Termination layer
5	Edge
6	Defect areas
7	Active area
72	Gate conductor structure
73	Transistor

[0028] In accordance with exemplary aspects of the present invention, Figure 4 provides exemplary structure of insulator trenches 21 introduced in a semiconductor substrate 1 and webs 22 formed from the monocrystalline silicon of the semiconductor substrate 1.

[0029] Firstly, insulator trenches 21 are introduced into the semiconductor substrate 1, which is covered with a protective layer 11, for instance a pad nitride, at least in the section under consideration. In this case, webs 22 provided with residual sections of the protective layer 11 are formed between the insulator trenches 21. In the exemplary embodiment depicted, the semiconductor substrate 1 is formed exclusively from monocrystalline silicon, in a simplified illustration. In actual fact, parts of capacitor or transistor structures have already been formed in the semiconductor substrate 1, so that the insulator trenches 21, in sections, may adjoin different materials than the monocrystalline silicon of the semiconductor substrate 1.

[0030] A nondoped silicon oxide layer is first deposited as additional layer 31 onto the exemplary structure in an HDP/CVD process chamber. Afterward, the invention provides for a barrier layer 32 to be produced by means of changing the precursor materials supplied in the same HDP/CVD process chamber, said barrier layer bearing on the additional layer 31. After the production of the barrier layer 32, the main layer 33 is deposited, once again by changing the precursor materials supplied. In this

exemplary embodiment, in this case the insulator trenches 21 are filled as far as an upper edge of the main layer 33 below the substrate surface 10. By once again simply changing the precursor materials supplied, a termination layer 34 is subsequently formed in situ in the HDP/CVD process chamber, and completes a filling 3 of the insulator trenches 21. The insulator structure 8 thus has the same properties as customary insulator structures for subsequent processing steps. Consequently, there is no need for any further adaptation of the subsequent processing steps to the insulator structure 8 according to the invention.

[0031] Figure 4 reveals the insulator filling 3 in the region of the insulator trenches 31, said insulator filling being composed of the additional layer 31, the barrier layer 32, the main layer 33 and the termination layer 34. The height of the webs 22 is about 320 nm and the thickness of the protective layer 11 is 130 nm.

[0032] Figure 5 illustrates the construction according to the invention in the area of an edge 5. In the area of the edge 5, the barrier layer 32 does not bear on the material of the semiconductor substrate 1, but rather remains isolated from the semiconductor substrate by the additional layer 31.

[0033] An insulator structure 8 processed according to a further exemplary embodiment of the method according to the invention is illustrated in Figure 6. The insulator trenches 21 have, at the opening, a width of about 200 nm and also a depth of about 300 nm. The webs 22 are covered by in each case approximately 150 nm thick residual sections of a protective layer 11.

[0034] Firstly, an approximately 100 nm thick additional layer 31 made of undoped silicon oxide is deposited onto the structure formed by the insulator trenches 21 and

the webs 22. The deposition is effected in a suitable process chamber with the precursors silane SiH4 and oxygen O2 being supplied. Directly after the deposition of the undoped silicon oxide, by changing the precursors supplied, a thin barrier layer 32 is produced in situ in the same process chamber. Once again directly after the deposition of the barrier layer 32, a fluorine-doped silicon oxide layer is produced in situ as main layer 33 by supplying the precursors silane SiH4, oxygen O2 and nitrogen trifluoride NF3. No defect areas with low-quality oxide are discernible in an SEM recording on which Figure 6 is modeled.

[0035] As an example, an application of a multilayer insulator filling in an HDP/CVD process chamber is achieved by provision of a source plasma, a first undoped deposition of an additional layer with a prestress according to a known type, a production of a barrier layer, a fluorine-doped deposition of a main layer, and an undoped deposition of a termination layer with a prestress.

[0036] Accordingly, aspects of the invention relate to providing a method for producing insulator structures by filling insulator trenches introduced into a semiconductor substrate, in which insulator trenches with a high aspect ratio are filled reliably and completely and a functionality of semiconductor devices that are subsequently formed in the semiconductor substrate remains ensured. Moreover, an insulator structure is provided which ensures a functional integrity of the semiconductor devices subsequently formed in the semiconductor substrate, in particular of p-channel transistors.

[0037] A method in accordance with aspects of the invention for producing insulator structures in a semiconductor substrate thus provide, an introduction of insulator

trenches into the semiconductor substrate from a substrate surface and a filling of the insulator trenches with a main layer made of an additive-doped insulator material in the course of an (HDP) deposition process based on a high density plasma. A barrier layer, which blocks an interaction of the additive with the semiconductor substrate, is produced in situ before a deposition of the main layer in the course of the HDP deposition process. This is because it could initially be observed that p-channel transistors that are formed using customary technology outside the insulator structures in the area of the substrate surface of the semiconductor substrate are subject to a progressive degradation if the p-channel transistors are formed in sections which are covered with a silicon nitride liner in a conventional manner before the HDP/CVD position process. Unexpectedly, however, a significantly reduced degradation was able to be established on otherwise identically formed p-channel transistors if a barrier layer – produced according to the invention – against an outgassing of the additives was provided instead of the silicon nitride liner.

[0038] It is assumed in this case that a property of the silicon nitride or barrier layer which is critical for a degradation of the p-channel transistors has its roots in the fabrication process itself or in the proximity of the fabrication process to further process steps. The barrier layer fabricated according to an aspect of the invention differs, for instance, from known plasma nitride layers typically by virtue of the close spatial and temporal relationship with a directly ensuing deposition of silicon oxide doped with an additive.

[0039] Furthermore, a relatively complicated processing is necessary for a removal of a conventional silicon nitride liner, since it generally also requires a removal of an

oxide layer connected to the silicon nitride liner, including an annealing step thus required. By contrast, in accordance with the invention, the barrier layer provided can be removed relatively simply together with the drawing-back of insulator material applied above the substrate surface.

[0040] Preferably, in the course of the HDP deposition process, directly after the production of the barrier layer, the additive-doped insulator material is deposited in a main deposition step and a main layer of the insulator structure is produced in this case.

[0041] The inventive method thus makes it possible, on the one hand, to fill insulator trenches with a high aspect ratio in a virtually ideal manner without the formation of defect areas characterized by low-quality oxide. The method makes it possible, moreover, to form p-channel transistors with a low tendency toward degradation in other sections of the semiconductor substrate. The effect observed is particularly advantageous if, in the course of the HDP deposition process, before the deposition of the barrier layer, a predeposition process is controlled with exclusion of halogens or halogen compounds and an additional layer of the insulator structure is provided in this case.

[0042] The additional layer effects, in a simple manner, an advantageous adaptation of the main layer or the barrier layer to the semiconductor substrate. A material or a composition of the additional layer is chosen such that interactions of the additional layer with the semiconductor substrate, for instance with regard to a constitution of the interface between additional layer and semiconductor substrate and also adhesion and diffusion properties are known and can be controlled in a simple manner. A

further adaptation of the semiconductor substrate to the properties of the main layer or the barrier layer is unnecessary. The additional layer is preferably formed from undoped silicon oxide. The thickness of the additional layer is chosen such that the semiconductor substrate is covered by it as far as possible completely at least in the region of the insulator trenches.

[0043] In a particularly advantageous manner, the predeposition process, in the course of which the additional layer is produced, the production of the barrier layer and the main deposition process, in the course of which the main layer is produced, are controlled successively and in situ in the same process chamber. Transitions between the additional layer and the barrier layer or between the barrier layer and the main layer are not exposed to any process environment other than a controlled one, so that no undefined interface surfaces are formed at the transitions. Rather, such a method is fast and enables a high throughput of semiconductor substrates.

[0044] A halogen or a halogen compound is preferably to be taken into consideration as the additive, it being possible for the halogen to act as an etching component in the course of an HDP/CVD deposition process. In an advantageous manner, fluorine is provided as the halogen, said fluorine emerging from nitrogen trifluoride NF3 as a chemical precursor compound (precursor).

[0045] Silicon oxide is preferably provided as the insulator material, the processing of said silicon oxide being known and well-controllable in a wide spectrum.

[0046] The advantages of the method according to the invention are manifested in particular when an insulator material deposited above the substrate surface during the HDP/CVD deposition process is caused to recede as far as the substrate surface in the

course of a subsequent etching process or CMP process. In known methods, in this case defect areas with low-quality oxide are uncovered within the insulator trenches, are caused to recede by the etching method and can subsequently be filled with conductive material in a disadvantageous manner. The formation of defect areas is avoided by the method according to the invention.

[0047] In particular when, after the formation of the insulator structures, p-channel transistors are formed in sections on the substrate surface outside the insulator structures, a particular advantage of the method according to the invention is that a rapid degradation of the p-channel transistors is prevented.

[0048] Silane and oxygen are then preferably supplied as chemical precursor compounds in the course of the predeposition process. Admixable inert gases in this case are Ar, He and H2.

[0049] During the main deposition process, according to a particularly preferred embodiment of the method according to the invention, silane, oxygen and nitrogen trifluoride NF3 are supplied as chemical precursor compounds. In contrast to customary methods in the course of which silicon tetrafluoride SiF4 is supplied as precursor compound for fluorine-doped silicon oxide, it is thus possible to set a fluorine proportion in the main layer of the insulator structure independently of the silicon proportion. Consequently, the additional process parameter obtained enables the properties of the fluorine-doped silicon oxide to be further adapted to process requirements.

[0050] The barrier layer is preferably formed from Si-N, Si-O-N, Si-C, Si-O-C, amorphous silicon and/or nitrided silicon oxide. In this case, a silicon nitride layer

produced according to the invention has significantly better properties than conventionally produced silicon nitride liners with regard to the formation of p-channel transistors in the semiconductor substrate.

[0051] The silicon nitride layer is preferably formed using the precursor compounds N2 and SiH4, it being possible additionally to add inert gases such as Ar, He and H2.

[0052] A use of the method according to the invention is advantageous particularly when the insulator structures emerge from the filling of insulator trenches which have an aspect ratio AR > 4:1.

[0053] The method according to the invention is used to produce an insulator structure according to the invention in a semiconductor substrate. The insulator structure initially comprises a main layer, which has been formed from a halogen-doped silicon oxide and has emerged from an HDP deposition process. According to the invention, the insulator structure has a barrier layer, which isolates the main layer from the semiconductor substrate. The barrier layer emerges from an HDP deposition process directly related to the formation of the main layer and prevents an interaction between halogen outgassing from the main layer and the semiconductor substrate.

[0054] In a particularly advantageous manner, an additional layer of the insulator filling is formed between the barrier layer and the semiconductor substrate.

[0055] The barrier layer preferably comprises Si-N, Si-C, Si-O-N, Si-O-C, amorphous silicon and/or nitrided silicon oxide. The materials mentioned are suitable for preventing an outgassing of a halogen, in particular of fluorine, from the doped silicon oxide. Furthermore, for the materials mentioned, suitable precursors are available for an HDP/CVD deposition process.

[0056] The insulator structure according to the invention is advantageous particularly when the insulator structure is arranged in an insulator trench whose aspect ratio AR is greater than 4:1. In the case of aspect ratios AR > 4:1, insulator structures formed at least partially from halogen-doped silicon oxide are distinguished by a comparatively small number of defects.

[0057] The foregoing disclosure of embodiments of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many variations and modifications of the embodiments described herein will be obvious to one of ordinary skill in the art in light of the above disclosure. The scope of the invention is to be defined only by the claims appended hereto, and by their equivalents.